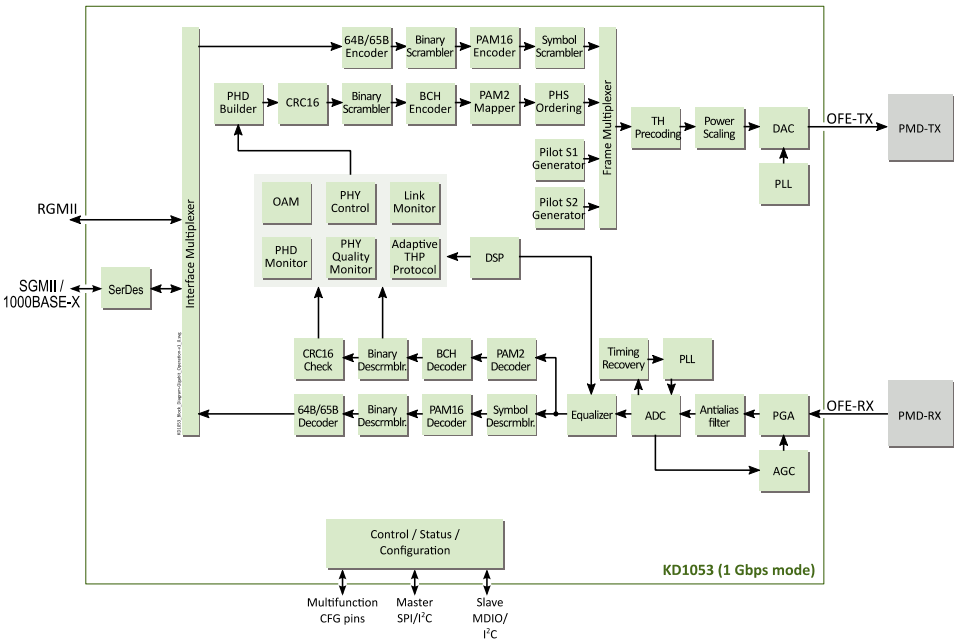
Product Brochure

KD1053

Automotive 1000BASE-H Transceiver

KD1000 FAMILY



OVERVIEW

The KD1053 is a 65nm CMOS ASIC that implements the Physical-Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer of a 1000BASE-RHx PHY, compliant with the specifications of IEEE Std 802.3bv™-2017 standard for gigabit optical communications over plastic optical fiber (POF). The KD1053 must be connected to a compatible Fiber Optics Transceiver (FOT), which implements a Physical Medium Dependent (PMD) sublayer and a Medium Dependent Interface (MDI), to form a complete automotive 1000BASE-RHC physical layer.
The KD1053 implements the following optional features of IEEE Std 802.3bv™-2017: 1000BASE-H Operations Administration Maintenance (OAM) channel, support for Energy Efficient Ethernet (EEE) mode, exposed Management Data Input/Output (MDIO) and motor vehicle environmental requirements.

The KD1053 can operate at 1 Gbps and at 100 Mbps. It is optimized for EMC compatibility, low power, reduced BOM and a small footprint. It is targeted for automotive applications using optical Ethernet over POF for the communications inside the vehicle. Infotainment and Advance Driver Assistance Systems (ADAS) are two of the key applications for future on board POF networking development. Examples of products able to incorporate optical Ethernet ports based on the KD1053 ASIC include ECUs, cameras and infotainment nodes

Its built-in analog interface simplifies connectivity to the Physical Medium Dependent (PMD) sublayer. It supports different parallel and serial MAC interfaces for connecting a MAC station, an MCU or a switch. The KD1053 transceiver provides a Serial Management Interface (SMI), also called MDC/MDIO interface, and master SPI/I2C port to access an external EEPROM memory for configuration.

The transceivers' parallel MAC interface pins are 1.8V, 2.5V and 3.3V LVTTL compliant; and serial MAC interfaces are 2.5V LVDS.

FEATURES

- **In 1 Gbps operation mode, 1000BASE-H Physical Coding Sub-layer (PCS) and the Physical Medium Attachment (PMA) sublayers according to the IEEE Std 802.3bv™-2017**
- **100 Mbps operation mode supported for applications requesting low data rates and high optical link margin**
- **Specified for multimode plastic optical fiber with the channel characteristics specified by IEEE Std 802.3bv™-2017 Clause 115. Designed to operate:**
  - **at 1 Gbps with the fiber optic channel type II and type III according to Clause 115 of IEEE Std 802.3bv™-2017;**
  - **at 100 Mbps with 120 m of SI-POF without in-line connectors, or with 40 m with up to 10 in-line connectors**
- **Support RGMII v2.0, RMII, MII, SGMII, 1000BASE-X and 100BASE-X standards in the MAC interface**
- **Support 1.8V 2.5V and 3.3V LVTTL digital I/O standard for parallel MAC interface; and 2.5V LVDS for serial MAC interface**
- **SMI (MDC/MDIO) interface for configuration and monitoring supporting Clauses 22 and 45, which can be configured as an I2C bus**
- **SPI/I2C master interface for reading external boot and configuration EEPROM memory**
- **Support for EEE, OAM, Wake-up & Sleep, interruption generation**
- **Support for jumbo packets up to 10 KB**
- **PTP and Sync-E supported**
- **Different loopback modes and PMD test-modes for diagnostics**
- **Link/activity monitoring and speed LED outputs**
- **Support for high-level ASIL systems**
- **Fully integrated digital adaptive non-linear equalizers**
- **BER < 10^{-12} for 1 Gbps and 100 Mbps operation modes**
- **6.2 us latency for 1 Gbps operation and 1.4 us for 100 Mbps (local RGMII to remote RGMII); 5 ns RMS jitter for 1 Gbps operation and 9 ns for 100 Mbps**
- **55 ms of link time for 1 Gbps operation**
- **Internal dependability functions: power supply, process and temperature sensors; and FOT received power monitoring**
- **Advanced power management with integrated linear voltage regulators for 2.5V: it can be supplied with only external 1.2V and 3.3V power voltages**
- **Low power, 460 mW at 1 Gbps**
- **Low-cost bill of materials (BOM)**
- **Designed to be EMC compliant with CISPR25 Class-5 at component level**
- **65 nm CMOS process**
- **Automotive AEC-Q100 grade 2**
- **-40 to +105ºC ambient temperature range**
- **56-pin QFN (7 x 7 mm) ROHS package**

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